REMARKS

Claims 1-13 stand rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,532,024 to Everett et al. (hereinafter "Everett et al."). The claims have been amended to more particularly define the present invention over the cited prior art.

More particularly, independent claims 1, 9 and 13 have been amended to recite that the input video signal, the background video signal and the output video signal are all of an interlaced format and that the background video signal (and consequently the output signal) is of a higher definition than the input video signal. The Everett et al. reference cited by the Examiner is different in that whereas the input signal is of interlaced format, the output signal is of a progressive format (i.e. non-interlaced format) for display on a non-interlaced computer monitor (see abstract).

The independent claims 1, 9 and 13 have been amended to make it clear that the input video signal, the background video signal and the output video signal all comprise two interlaced fields. The claimed video processors include combining circuitry for superimposing a re-sized picture component signal and a measurement component signal, both derived from and consequently of the same interlaced format and definition as the input signal, onto a carrier or background signal of a second higher definition and also of interlaced format. This produces an output video signal of the second higher definition comprising two interlaced fields. This provides a convenient way for displaying for

example, a standard definition 720x576 interlaced picture on part of a high definition 1 920x 1080 interlaced display.

In contrast, the system of Everett et al. does not superimpose a lower definition interlaced format signal onto a higher definition interlaced format signal; instead, a standard definition interlaced signal input to the system is converted into progressive format (i.e. non-interlaced format) for display on a computer monitor. To this end, the system of Everett et al. comprises a video line doubler (100), prior to re-sizing engine (102), the line doubler (100) for converting from interlaced to non-interlaced format (see column 6 lines 10 to 19). The non-interlaced signal is then input to the re-sizing engine 102 for processing for display on the non-interlaced monitor. Thus in the system of Everett et al., a picture component of an interlaced input signal of a first definition is not simply superimposed on a background interlaced signal of a higher definition as required by the amended claims. Everett et al. thus does not disclose the video signal generator or the combining circuitry defined in the independent claims 1, 9 and 13.

In the system of Everett et al., the processing involved in dc-interlacing the signals causes loss of quality in the displayed picture. Advantageously, the video processor of the present invention overcomes this problem.

The dependent claims 2-8 and 10-12 are patentable over the cited prior art for those reasons advanced above with respect to independent claims 1 and 9 from which they respectfully depend and for reciting additional features that are neither taught nor

suggested by the cited prior art. For example, claim 3 recites that "the first definition comprises a first plurality of horizontal lines per frame and the second definition comprises a second plurality of horizontal lines per frame **higher than** the first plurality of horizontal lines per frame." Nowhere does the cited prior art teach or suggest this feature.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,

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